IN THE SPECIFICATION

Applicants acknowledge that the Examiner has objected to the specification filed on September 22, 2003. Pursuant to these objections, the following amendments have been made to the specification:

On page 11, line 24 – page 12, line 20, please amend the paragraph as follows:

The comparators 410, 411, 412 are arranged to assert a signal in response to the temperature dependent voltage V_{temp} on the line 403 exceeding the reference ~~voltage~~ voltages V1, V2, V3 to which the comparators 410, 411, 412 are coupled. For example, when the temperature dependent voltage V_{temp} on the line 403 is more than all three of the reference voltages V1, V2, V3, all of the comparators 410, 411, 412 will assert a signal at their output terminals. Thus, the three asserted signals indicate that the temperature of the memory array 210 is less than the first setpoint temperature T1. As the temperature rises above T1, the temperature dependent voltage V_{temp} on the line 403 falls below the first reference voltage V1 coupled to the comparator 410, but remains ~~below~~ above the second and third reference voltage levels V2, V3 coupled to the comparators 411, 412. Thus, the output terminal of the comparator 410 is unasserted, whereas the output terminals of the comparators 411, 412 remain asserted, indicating that the temperature of the memory array 210 is greater than T1. As the temperature of the memory array 210 rises above a second setpoint temperature T2, the temperature dependent voltage V_{temp} on the line 403 will be less than the second reference voltage V2 coupled to the comparator 411, but remains above the third reference voltage V3 coupled to the comparator 412. Thus, the output terminal of the comparators 410, 411 are unasserted, whereas the output

terminal of the comparator 412 remains asserted, indicating that the temperature of the memory array 210 is greater than T2. Finally, as the temperature of the memory array 210 rises above a third setpoint temperature T3, the temperature dependent voltage V_{temp} on the line 403 will be lower than the third reference voltage V3 coupled to the comparator 412. Thus, the output terminals of the comparators 410, 411, 412 are all unasserted, indicating that the temperature of the memory array 210 is greater than T3.

On page 15, lines 13 – 22, please amend the paragraph as follows:

Turning now to Figure 6A a transistor level schematic for an exemplary embodiment of a comparator 600 that may be used for any of the comparators 410, 411, 412 of Figure 4 is shown. A first portion of the circuit is a preamplification circuit, which may take the form of a differential amplifier with active loads 603, 604. The signals V_{temp} and V_{ref} are electrically coupled to the bases of a pair of PMOS type ~~transistor~~ transistors 601, 602, respectively. The transistors 601, 602 are in turn respectively serially coupled to a pair of NMOS type transistors 603, 604, which are configured as diodes. Both sets of serially connected transistors 601, 603; 602, 604 are coupled between a voltage supply V and ground through control transistors 605, 606. The transistor 605 is used to provide a bias current. The transistor 606 is used to selectively enable operation of the comparator 600 at desired time intervals.

On page 15, line 24 – page 16, line 6, please amend the paragraph as follows:

The second part of the circuit, which comprises transistors 607-613, constitute a decision making portion of the circuit. The current flowing through transistors 603, 604 is mirrored into the transistors 607, 608 depending upon the relative voltage levels of the signals V_{temp} and V_{ref}. The transistors 607, 608 are each coupled in series with a pair of parallel arranged transistors

609, 610; 611, 612. The transistors 607-612 are coupled between a voltage source V and ground by the control transistor 606 and a transistor ~~614~~ 613 configured as a diode. This circuit uses a cross coupled connection between transistors 610, 611 to increase the gain of the circuit.

On page 15, lines 13 – 22, please amend the paragraph as follows:

Turning now to Figure 6B, a transistor level schematic for an exemplary embodiment of a selected portion of the digital filter 440 of Figure 4 is shown. The portion of the digital filter 440 illustrated in Figure 4B may be replicated four times with each replicated portion being coupled to one of the lines 431, 432, 433, 434 from the digital circuit 430 of Figure 4. The digital filter 440 includes four transistors 650, 651, 652, 653 serially connected between a voltage supply V and ground. The transistors 650, 653 are respectively a PMOS and an NMOS type transistor, and both have their bases coupled to receive a control signal, SAMPFILTER. The transistors 651, 652 are both NMOS type transistors with their bases respectively coupled to receive the last two temperature signals, ~~TEMP1~~ TEMP2 and ~~TEMP2~~ TEMP1 generated on the corresponding line 431, 432, 433, 434 from the logic circuit 430. The TEMP1 and TEMP2 signals may be derived from a pair of serially connected flip flops or latches (not shown) that are clocked at a frequency approximately twice the frequency associated with the SAMPFILTER signal. Thus, each time the SAMPFILTER signal transitions, the flip flops will have received and stored the last two temperature signals over, for example the line 431.

On page 18, lines 18 – 22, please amend the paragraph as follows:

Thus, those skilled in the art will appreciate that the illustrated circuitry requires two consecutive temperature signals, TEMP1 and TEMP2, to be logically "high" before the digital

filter 440 will produce a corresponding output signal. Additionally, those skilled in the art will appreciate that the number of consecutive signals may be varied by correspondingly varying the number of transistors ~~451, 452~~ 651, 652 and their corresponding flip flops (not shown).

On page 18, line 24 – page 19, line 8, please amend the paragraph as follows:

Figure 7 illustrates a block diagram of an alternative embodiment of the temperature sensor 320. The embodiment of the temperature sensor 320 illustrated in Figure 7 is similar in certain aspects to the embodiment of the temperature sensor 320 illustrated in Figure 4. Thus, where like components are present, like reference numerals are employed. As discussed above, the band gap reference 415 produces three relatively temperature-independent voltages V1, V2, V3 on the lines ~~415,~~ 416, 417 418, respectively. In this embodiment, however, the lines ~~415,~~ 416, 417 418 are coupled to a multiplexer 700, which controllably delivers the reference voltage on each of the lines ~~415,~~ 416, 417 418 to its output terminal 701. Control and timing of the multiplexer 700 is accomplished by timing signals S1, S2, S3, discussed in more detail below in conjunction with Figure 8.

In view of the amendments set forth herein, reconsideration of the present application is respectfully requested of the Examiner.